1. 4 bytes of data transfer takes 4 μsec

2048 bytes of data transfer takes = 2048 μsec = 2.048 ms

1. CPU talks to the memory at the rate of 2 million instructions per sec.

ie , in 1 sec 2M x 32 bits = 64 M bits /s

Whereas, the DMAC is talking to the MM at 76800 bps.

This means that the DMA is slowing down the communication of CPU and MM.

Therefore, % of Slowdown .= 76800/64M x100%

1. CPU talks to the memory at the rate of 1 million instructions per sec.

Each instruction is 4 bytes.

CPU-MM transfer happens in 4M bytes / sec

Whereas, the DMAC to MM transfer happens with 2400 bytes/sec.

This communication affects the CPU-mem communication and results in a slowdown

So Percentage of slowdown = 2400/ 4M x 100%

1. Data transfer rate between I/O device and memory = 8KB/s

Overhead for every byte of transfer = 100+8 μsec

Total time spent in interrupt handling = 8192 x 108 μsec = 0.8 sec

This part of the CPU time is consumed by the interrupt driven I/O,

Fraction of CPU time consumed = 0.8/1 x 100% = 80%

1. 16 surfaces

512 tracks per surface

512 sectors per track

1024 bytes per sector

Therefore, the Total capacity = 16 x 512 x 512 x 1024 bytes

= 4 GB

Roration = 3600 rpm

Every DMA cycle = 4 byts

Memory access time is 40 ns

One track data is transferred at a time, one track = 512 x 1024 = 512 KB

3600 rotation in 60 sec

1 rotation in 1/60 sec

Therefore Data rate = 512 KBps / (1/60) = 30 MB/s

At the memory end,

In 40 ns there is a transfer of 4 Bytes

Therefore in 1 sec, 4/40ns = 100 MB of data can be transferred.

So the % of the CPU getting blocked is 30/100 x100 % = 30 %

1. Processor frequency 50 MHz.

Therefore, Clock Cycle Time = 1/f = 20 nsec

Now DMA setup time is = 2000 clock cycles = 2000 x 20 ns = 40 μsec

DMA completion overhead = 1000 clocks = 20 μsec

DIsk transfer rate = 4000 KB/s

Time taken for transfer of a block of data ie, 8 KB = 8/4000 s = 2 ms

Now the total time taken for transfer of 8KB = 2 ms + 40 μsec + 20 μsec

= 2.06 ms

In ideal scenario, cpu transfer happens all the times.

Data transfer information between the processor and memory is missing for this question, which makes the next part of the question inconclusive.

1. A device has a data transfer rate of 20 KB/sec

Interrupt overhead 6 μsec

So in second of data transfer, the total overhead incurred is 6 x 10^-6 x 20 x 10^3

= 120ms

So in 1sec, ie, 1000 msec, 120ms of the time is spent data transfer.

Thus, the performance gain = (1000 - 120)/ 100 %